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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY.DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/654,542	09/02/2003	1753	503	NT-260-US	4	27	3

Legal Department
NuTool, Inc
1655 McCandless Drive
Milpitas, CA 95035

CONFIRMATION NO. 3972

UPDATED FILING RECEIPT

OC000000012055391

Date Mailed: 03/09/2004

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

Bulent M. Basol, Manhattan Beach, CA;
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Domestic Priority data as claimed by applicant

This appln claims benefit of 60/407,449 08/30/2002

Foreign Applications

If Required, Foreign Filing License Granted: 11/21/2003

Projected Publication Date: 06/17/2004

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

Constant low force wafer carrier for electrochemical mechanical processing and chemical mechanical polishing

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Basol et al. Serial No.: 10/654,542 Filed: September 2, 2003 Title: Constant Low Force Wafer Carrier For Electrochemical Mechanical Processing And Chemical Mechanical Polishing	Group Art Unit: 1753 Examiner: Not yet assigned Docket: NT-260-US CERTIFICATE OF MAILING I hereby certify that this correspondence is being deposited with the US Postal Service as First Class Mail in a postage-paid envelope addressed to the Commissioner for Patents, P.O. BOX 1450, Alexandria, VA 22313-1450 on April 1, 2004. Signed: _____ Amy Alwine

REQUEST FOR CORRECTED FILING RECEIPT

Commissioner for Patents
P.O. BOX 1450
Alexandria, VA 22313

Dear Sir:

In response to receipt of the Filing Receipt, submitted herewith are a copy of the Filing Receipt and first page of the above-identified application that indicates a claim of priority to U.S. Serial No. 10/155,828, which is not shown on the Filing Receipt. Applicants respectively request that the Filing Receipt be updated to indicate the claim of priority to U.S. Serial No. 10/155,828 filed May 23, 2002 and U.S. provisional application 60/407,499.

If any matters can be resolved by telephone, Applicants request that the Patent and Trademark Office calls the Applicants at the telephone number listed below.

Respectfully submitted,

By: _____
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EL452444924US

CONSTANT LOW FORCE WAFER CARRIER FOR ELECTROCHEMICAL MECHANICAL PROCESSING AND CHEMICAL MECHANICAL POLISHING

INVENTORS: BULENT M. BASOL, JALAL ASHJAEE, KONSTANTIN VOLODARSKY

RELATED APPLICATIONS

[0001] This application claims the priority of U.S. Ser. No. 10/155,828 filed May 23, 2002 (NT-226) and prior U.S. provisional application 60/407,449, filed August 30, 2002, all incorporated herein by reference.

FIELD

[0002] The present invention relates generally to semiconductor integrated circuit manufacturing technology and, more particularly, to processing apparatus and processing techniques such as electroplating, electroetching and chemical mechanical polishing that are applied to a workpiece surface.

BACKGROUND OF THE INVENTION

[0003] Conventional semiconductor devices generally include a semiconductor substrate, such as a silicon substrate, and a plurality of sequentially formed dielectric interlayers such as silicon dioxide and conductive paths or interconnects made of conductive materials. Copper and copper alloys have recently received considerable attention as interconnect materials because of their superior electro-migration and low resistivity characteristics. The interconnects are usually formed by filling copper in features or cavities etched into the dielectric layers by a metallization process. The preferred method of copper metallization is electroplating. In an integrated circuit, multiple levels of interconnect networks laterally extend with respect to the substrate surface. Interconnects formed in sequential layers can be electrically connected using vias or contacts.

[0004] In a typical process, first an insulating layer is formed on the semiconductor substrate. Patterning and etching processes are performed to form features such as trenches and vias in the insulating layer. Then, barrier and seed layers are deposited in the features and on the surface regions between the features formed. Afterwards, a conductor such as copper is electroplated to fill all the features. However, the plating process results in a thick copper layer on the substrate, some of which need to be removed before the subsequent step. Conventionally, after the copper plating,